

# DATA SHEET

**74ABT16500C**

**74ABTH16500C**

**18-bit universal bus transceiver (3-State)**

Product specification  
Supersedes data of 1997 Jun 12  
IC23 Data Handbook

1998 Feb 27

# 18-bit universal bus transceiver (3-State)

## 74ABT16500C 74ABTH16500C

### FEATURES

- 18-bit bidirectional bus interface
- 3-State buffers
- 74ABTH16500C incorporates bus-hold data inputs which eliminate the need for external pull-up resistors to hold unused inputs
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- Negative edge-triggered clock inputs
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Flexible operation permits 18 embedded D-type latches or flip-flops to operate in clocked, transparent, or latched modes.

### DESCRIPTION

The 74ABT16500C is a high-performance BiCMOS Device which combines low static and dynamic power dissipation with high speed and high output drive.

This device is an 18-bit universal transceiver featuring non-inverting 3-State bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $\overline{OEAB}$  and  $\overline{OEBA}$ ), latch enable ( $\overline{LEAB}$  and  $\overline{LEBA}$ ), and clock ( $\overline{CPAB}$  and  $\overline{CPBA}$ ) inputs. For A-to-B data flow, the device operates in the transparent mode when  $\overline{LEAB}$  is High. When  $\overline{LEAB}$  is Low, the A data is latched if  $\overline{CPAB}$  is held at a High or Low logic level. If  $\overline{LEAB}$  is Low, the A-bus data is stored in the latch/flip-flop on the High-to-Low transition of  $\overline{CPAB}$ . When  $\overline{OEAB}$  is High, the outputs are active. When  $\overline{OEAB}$  is Low, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B but uses  $\overline{OEBA}$ ,  $\overline{LEBA}$  and  $\overline{CPBA}$ . The output enables are complimentary ( $\overline{OEAB}$  is active High, and  $\overline{OEBA}$  is active Low).

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Two options are available, 74ABT16500C which does not have the bus-hold feature and 74ABTH16500C which incorporates the bus-hold feature.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Bn or Bn to An	$C_L = 50\text{pF};$ $V_{CC} = 5\text{V}$	2.1 1.7	ns
$C_{IN}$	Input capacitance (Control pins)	$V_I = 0\text{V}$ or $V_{CC}$	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O} = 0\text{V}$ or $V_{CC}$	7	pF
$I_{CCZ}$	Quiescent supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	$\mu\text{A}$
$I_{CCL}$		Outputs low; $V_{CC} = 5.5\text{V}$	8	mA

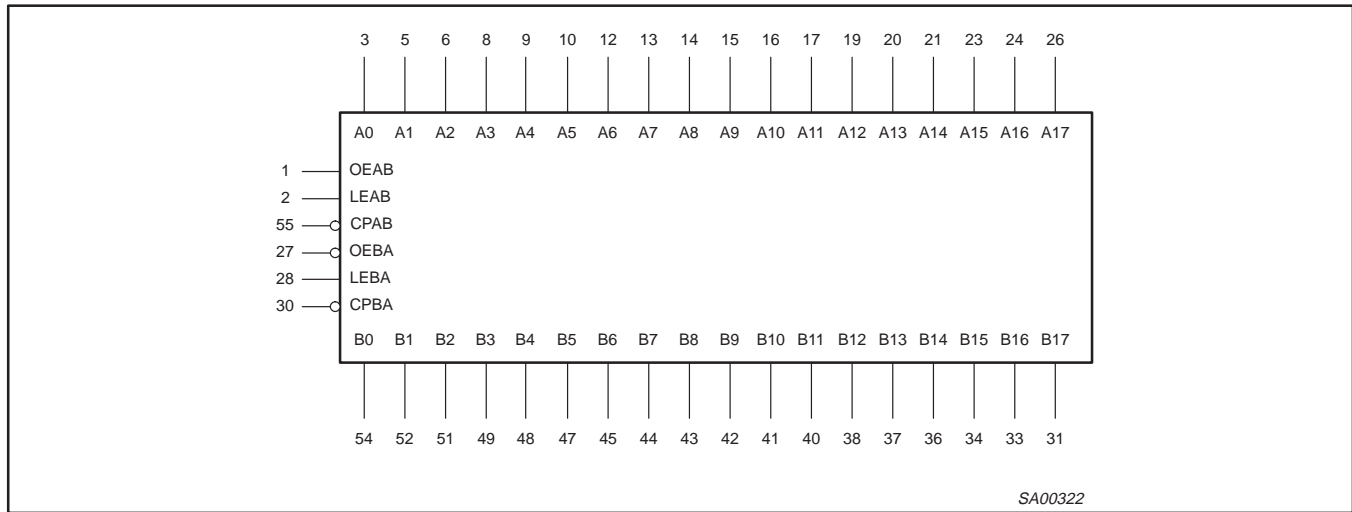
### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ABT16500C DL	BT16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABT16500C DGG	BT16500C DGG	SOT364-1
56-Pin Plastic SSOP Type III	-40°C to +85°C	74ABTH16500C DL	BH16500C DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ABTH16500C DGG	BH16500C DGG	SOT364-1

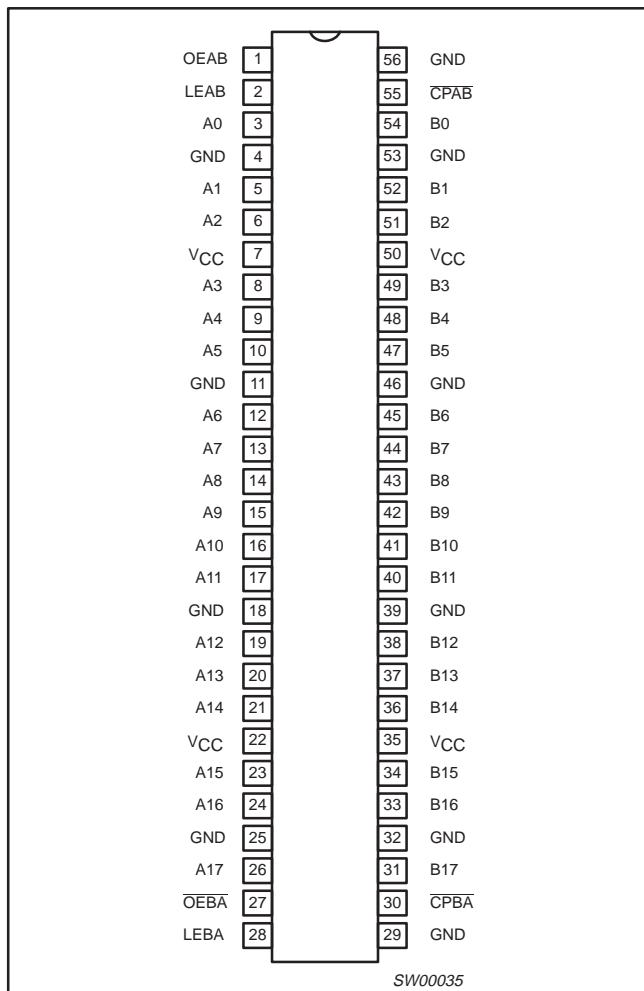
# 18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C

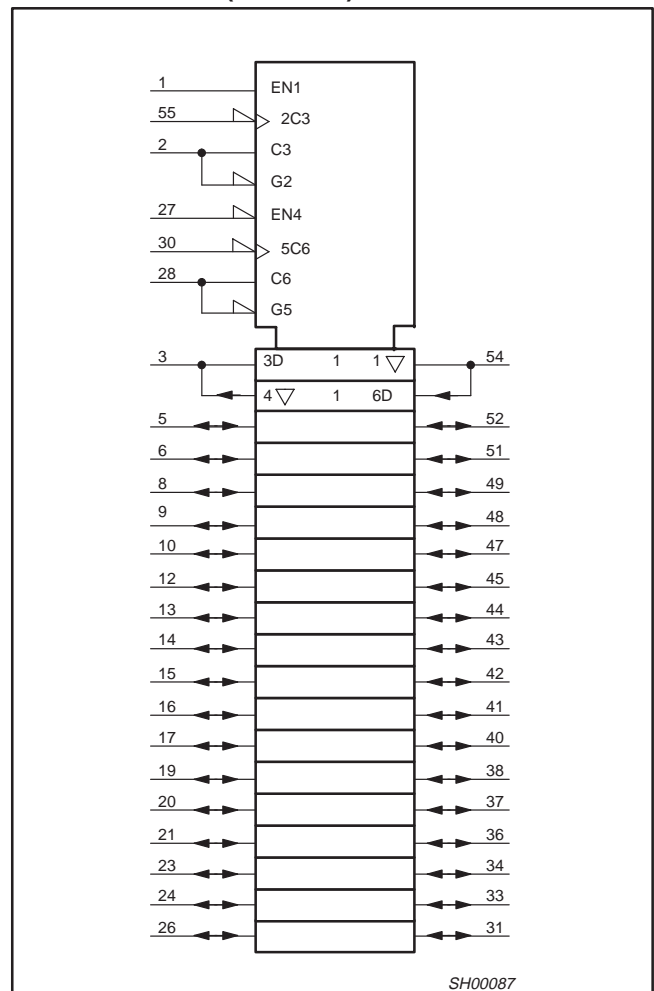
## LOGIC SYMBOL



## PIN CONFIGURATION



## LOGIC SYMBOL (IEEE/IEC)



## 18-bit universal bus transceiver (3-State)

74ABT16500C  
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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	A-to-B Output enable input
27	$\overline{OEBA}$	B-to-A Output enable input (active low)
2, 28	LEAB/LEBA	A-to-B/B-to-A Latch enable input
55,30	$\overline{CPAB/CPBA}$	A-to-B/B-to-A Clock input (active falling edge)
3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26	A0-A17	Data inputs/outputs (A side)
54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31	B0-B17	Data inputs/outputs (B side)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS				Internal Registers	OUTPUTS	OPERATING MODE
OEAB	LEAB	$\overline{CPAB}$	A <sub>n</sub>		B <sub>n</sub>	
L	H	X	X	X	Z	Disabled
L	↓	X	h	H	Z	Disabled, Latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	Disabled, Hold data
L	L	↓	h	H	Z	Disabled, Clock data
L	L	↓	l	L	Z	
H	H	X	H	H	H	Transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	Latch data & display
H	↓	X	l	L	L	
H	L	↓	h	H	H	Clock data & display
H	L	↓	l	L	L	
H	L	H or L	X	H	H	Hold data & display
H	L	H or L	X	L	L	

**NOTE:** A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{OEBA}$ , LEBA, and  $\overline{CPBA}$ .

H = High voltage level

h = High voltage level one set-up time prior to the Enable or Clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Enable or Clock transition

NC= No Change

X = Don't care

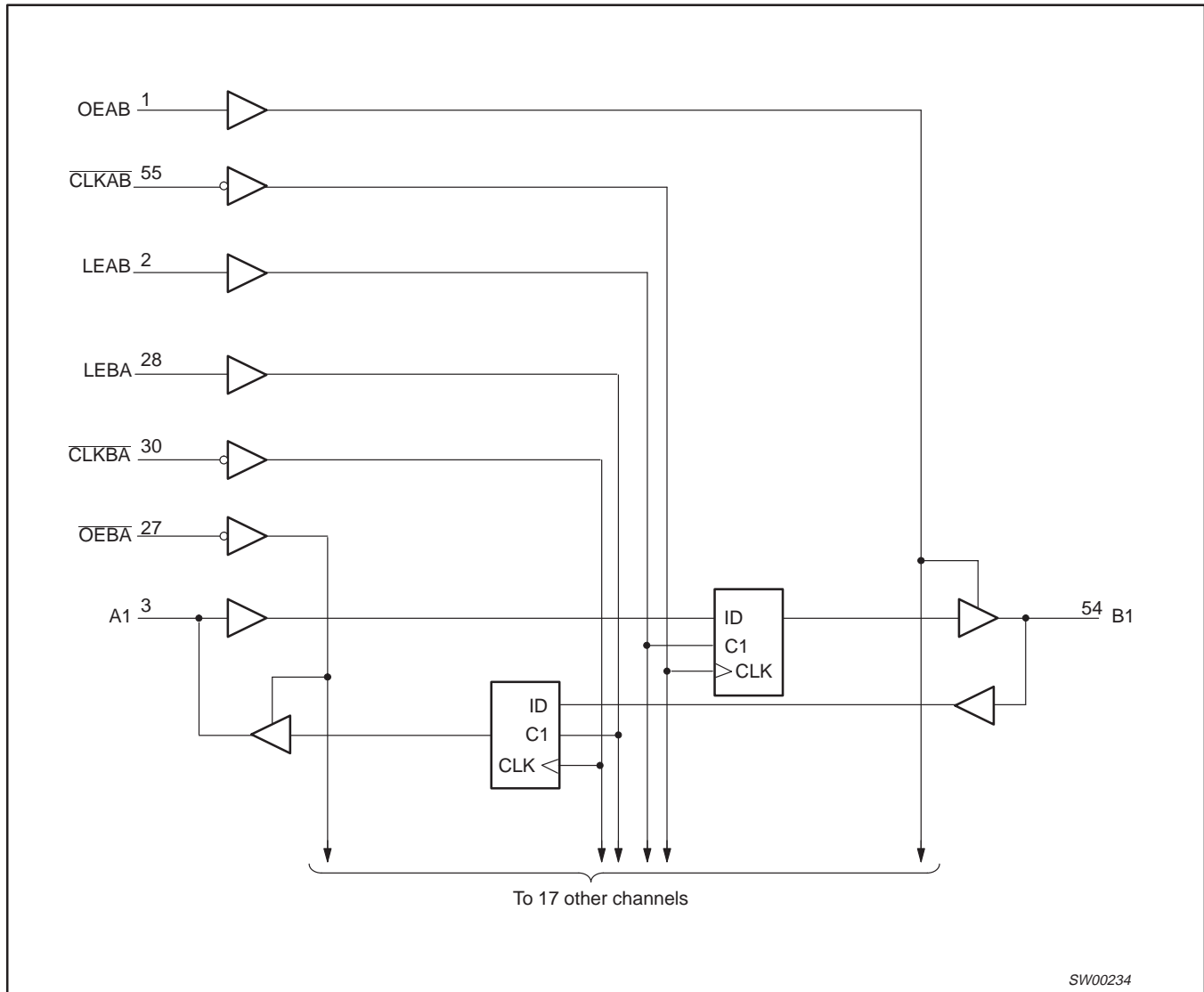
Z = High Impedance "off" state

↓ = High-to-Low Enable or Clock transition

# 18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C

## LOGIC DIAGRAM



SW00234

## 18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T <sub>stg</sub>	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## 18-bit universal bus transceiver (3-State)

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT	
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C			
			MIN	TYP	MAX	MIN	MAX		
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.8	-1.2		-1.2	V	
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V	
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	4.0		3.0		V	
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V	
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.35	0.55		0.55	V	
V <sub>RST</sub>	Power-up output voltage <sup>3</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V	Control pins		±0.01	±1.0		±1.0	μA
I <sub>HOLD</sub>	Bus Hold current A and B Ports <sup>6</sup> 74ABTH16500C	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0.8V	35			35		μA	
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 2.0V	-75			-75			
		V <sub>CC</sub> = 5.5V; V <sub>I</sub> = 0 to 5.5V	±800						
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±2	±100		±100	μA	
I <sub>PU/PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.0V or V <sub>CC</sub> ; V <sub>OE</sub> = Don't care		±2	±50		±50	μA	
I <sub>IH</sub> + I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		1.0	10		10	μA	
I <sub>IL</sub> + I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.0V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-1.0	-10		-10	μA	
I <sub>CEX</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		2	50		50	μA	
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V		-50	-80	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	2		2	mA	
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		8	19		19	mA	
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	2		2	mA	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup> 74ABT16500C	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		5.0	50		50	μA	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup> 74ABTH16500C	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		200	500		500	μA	

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
- This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V, with a transition time of up to 10msec. From V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10% a transition time of up to 100μsec is permitted.
- Unused pins at V<sub>CC</sub> or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

# 18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C

## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$	Maximum clock frequency	1	150	225		150		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Bn or Bn to An	2	1.0 1.0	2.1 1.7	3.0 2.5	1.0 1.0	3.4 3.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay LEAB to Bn or LEBA to An	3	1.0 1.0	3.2 2.8	4.3 3.7	1.0 1.0	4.9 4.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CPAB to Bn or CPBA to An	1	1.0 1.0	3.4 2.6	4.5 3.5	1.0 1.0	5.3 4.6	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to HIGH and LOW level	5 6	1.0 1.5	3.3 2.4	4.4 3.2	1.0 1.5	5.0 3.9	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from HIGH and LOW level	5 6	1.5 1.4	3.3 2.5	4.3 3.3	1.5 1.4	5.3 3.9	ns

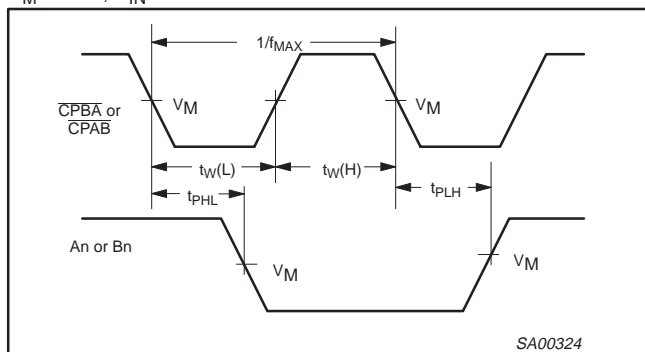
## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

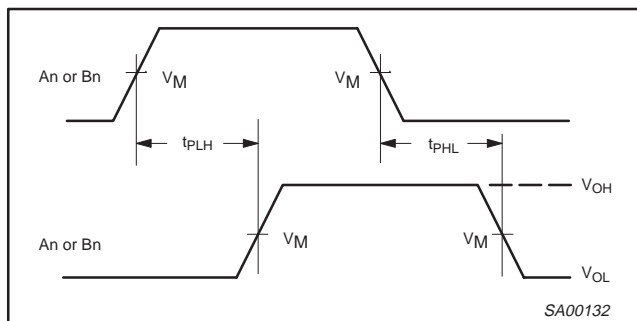
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$		$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$	
			MIN	TYP	MIN	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, HIGH or LOW An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	2.0 2.0	0.7 0.6	2.0 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, HIGH or LOW An to $\overline{\text{CPAB}}$ or Bn to $\overline{\text{CPBA}}$	4	0.7 0.7	-0.5 -0.8	0.7 0.7	ns
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, HIGH or LOW An to LEAB or Bn to LEBA	4	2.0 2.0	0.1 0.1	2.0 2.0	ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time HIGH or LOW An to LEAB or Bn to LEBA	4	0.7 0.7	-0.1 -0.1	0.7 0.7	ns
$t_w$	Pulse width, HIGH or LOW $\overline{\text{CPAB}}$ or $\overline{\text{CPBA}}$	1	3	1.2	3	ns
$t_w(\text{H})$	Pulse width, HIGH LEAB or LEBA	3	3	1.2	3	ns

## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Propagation Delay, Transparent Mode

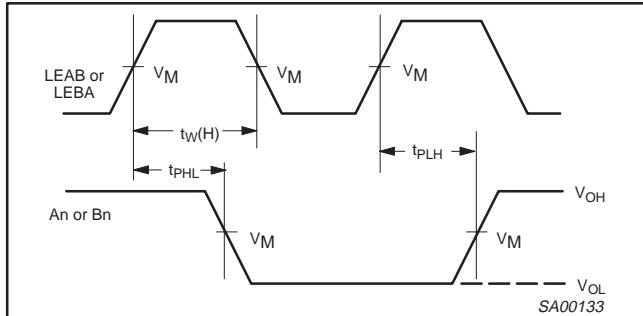


# 18-bit universal bus transceiver (3-State)

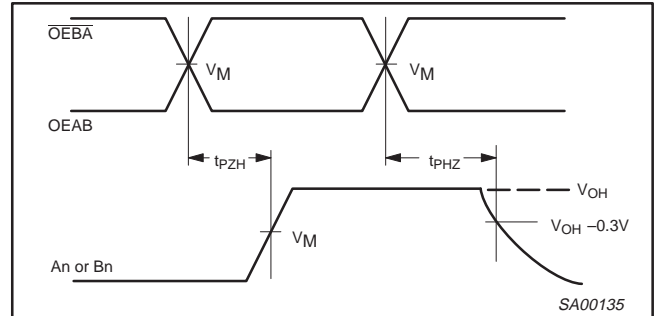
74ABT16500C  
74ABTH16500C

## AC WAVEFORMS (Continued)

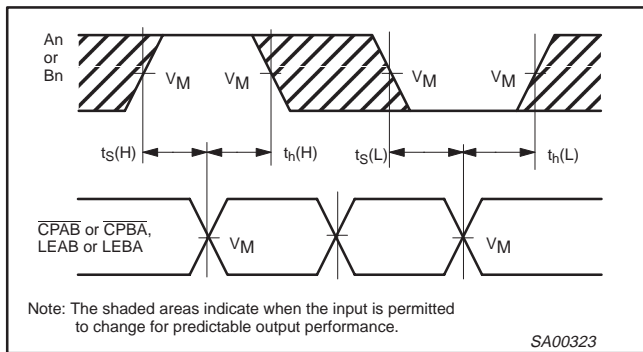
$V_M = 1.5V$ ,  $V_{IN} = GND$  to  $3.0V$



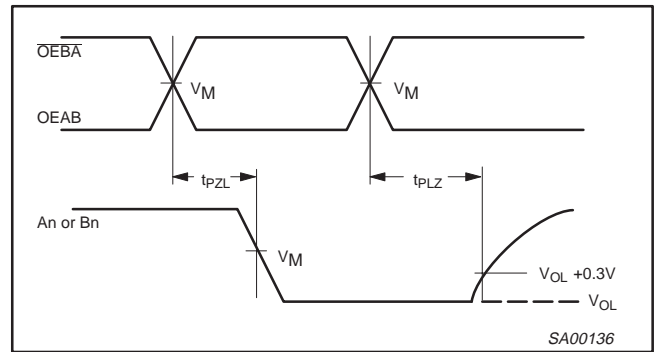
**Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width**



**Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level**



**Waveform 4. Data Setup and Hold Times**



**Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level**

## TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

**DEFINITIONS**

$R_L$  = Load resistor; see AC CHARACTERISTICS for value.  
 $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.  
 $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

$V_M = 1.5V$   
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	$t_w$	$t_R$	$t_F$
74ABT/H16	3.0V	1MHz	500ns	2.5ns	2.5ns

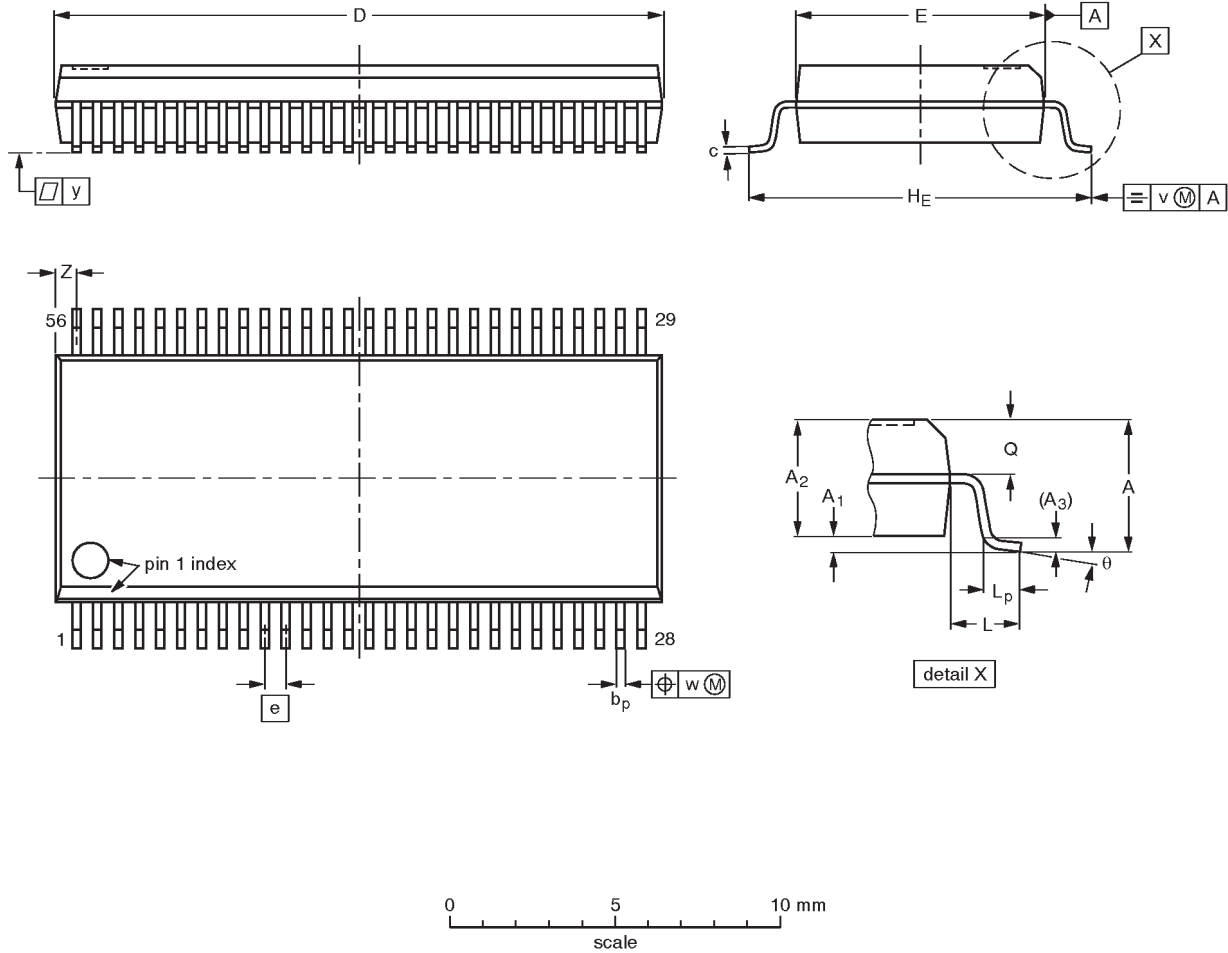
SA00018

18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

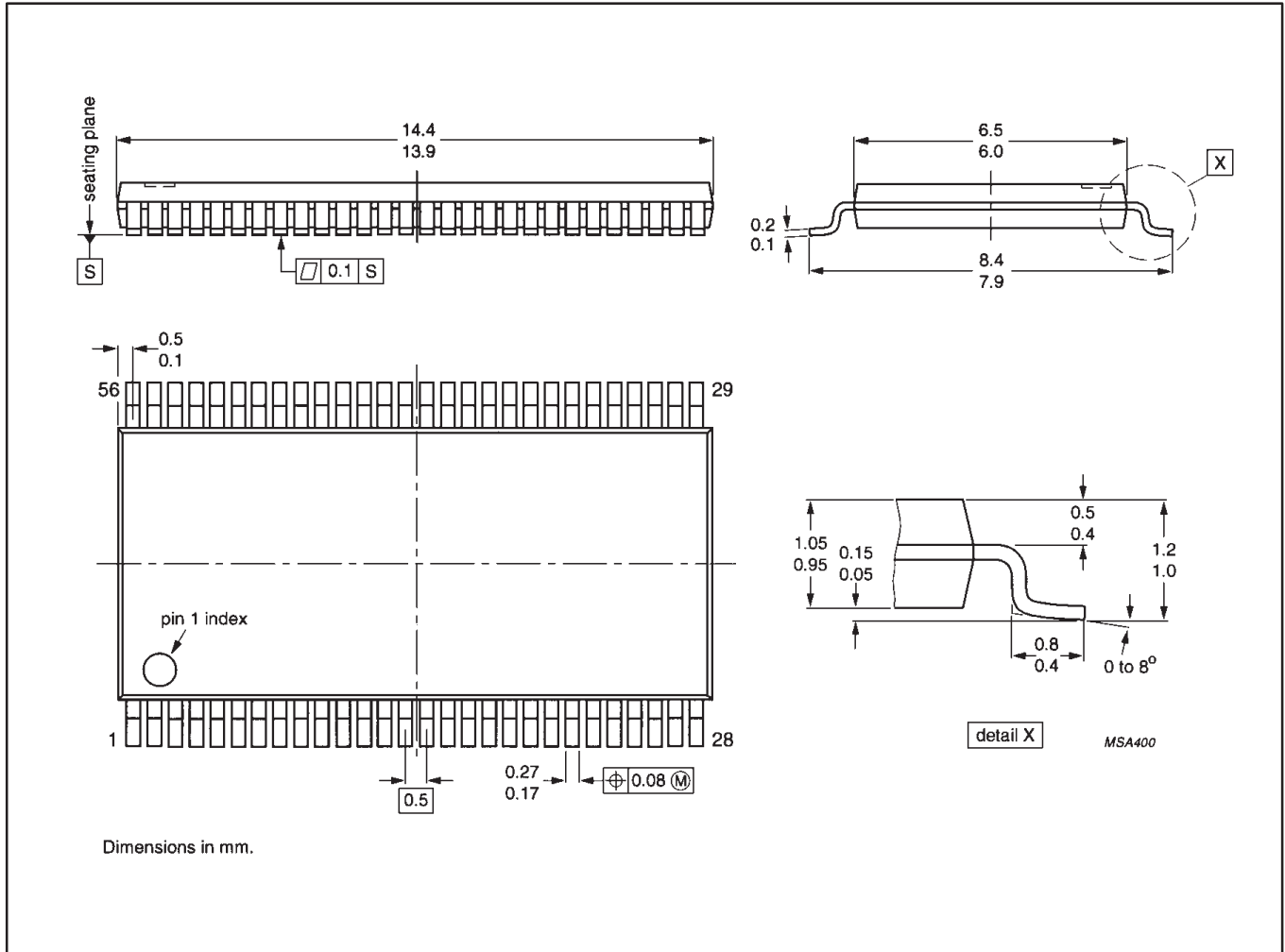
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

# 18-bit universal bus transceiver (3-State)

74ABT1650C  
74ABTH1650C

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



## 18-bit universal bus transceiver (3-State)

74ABT16500C  
74ABTH16500C

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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